REMARKS

The claims are claims 1 to 18.

Claims 1, 3, 7, 10, 12, and 16 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Shiell et al U.S. Patent Number 5,961,632 and O'Connor U.S. Patent Number 5,848,288.

Claims 1 and 10 recite subject matter not made obvious by the combination of Shiell et al and Connor. Claims 1 and 10 each recite "the fetch packet having an operating mode in dependence upon the execution mode at the time the request was made to the memory for the fetch packet." The FINAL REJECTION fails to point out any portion of Shiell et al disclosing the selection of operating mode based upon the claimed fetch packets. Shiell et al teaches at column 4, line 27 to column 6, line 37 and illustrated in Figures 2a and 2b that mode is dependent upon an instruction leading code. This differs from a current execution mode when the fetch packet is fetched from memory as recited in claims 1 and 10. Since both claims 1 and 10 recite simultaneous fetching of plural instructions, setting the mode by an instruction leading code as disclosed in Shiell et al is inappropriate. For example, two different instructions fetched at the same time could include conflicting instruction leading codes. Accordingly, claims 1 and 10 are allowable over Shiell et al.

Claims 2, 4 to 6, 8 to 9, 11, 13 to 15, 17 and 18 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Shiell et al U.S. Patent Number 5,961,632, O'Connor U.S. Patent Number 5,848,288 and Nishioka et al U.S. Patent Number 6,401,190.

Claims 2 and 11 recite subject matter not made obvious by the combination of Shiell et al, Connor and Nishioka et al. Claim 2 recites "a third input to said multiplexer wherein said third input is a no operation machine word." Similarly, claim 11 recites "choosing between the output of said migrant architecture decode

and the output of said base architecture decode input and a no operation machine word." Respective base claims 1 and 10 make clear that the machine words result from decoding of individual instructions in the base mode or migrant mode. Nishioka et al fails to disclose these machine words. The nop fields illustrated in Figures 5 and 6 of Nishioka et al are instructions within the original or expanded execute packet and not the no operation machine word claimed. Note that Nishioka et al fails to disclose the decoding of instructions into machine words as claimed. Figure 1 of Nishioka et al shows supply of instruction words stored in instruction registers 14 to 21 to respective computing units 23 to 25. Presumably the decode of instructions into machine words takes place within computing units 23 to 25 of Nishioka et al. The FINAL REJECTION fails to point out where Nishioka et al discloses or makes obvious the multiplexer selecting between the three machine words recited in claim 2 or the selection from three machine words recited in claim 11. Thus, even if the nop instructions of Nishioka et al were the no operation machine word recited in claims 2 and 11, the combination of Shiell et al, Connor and Nishioka et al fails to make obvious the selection among three machine words recited in claims 2 and 11. Accordingly, claims 2 and 11 are allowable over the combination of Shiell et al and Nishioka et al.

Claims 8 and 18 recite subject matter not made obvious by the combination of Shiell et al, Connor and Nishioka et al. Claim 8 recites "said migrant architecture control circuit for issuing no-operation instruction to preserve the semantics of the instruction in the migrant architecture." Similarly, claim 18 recites "issuing no-operation instruction from said migrant architecture control circuit, to preserve the semantics of the instructions in the migrant architecture." Nishioka et al teaches provision of nop instructions for a different purpose than recited

in claims 8 and 18. Nishioka et al states at column 28, lines 40 to 45:

> "Normally, in VLIW, about 80% of the objects is occupied by NOP. Therefore, NOP compression is an essential technology when memory usage efficiency is taken into consideration. Use of the header used by this technology also in the SIMD mode mitigates the overhead, which is the feature of this embodiment."

This portion of Nishioka et al states that nops are inserted for compression and memory usage. This is not the "to preserve the semantics of the instruction in the migrant architecture" as recited in claims 8 and 18. Accordingly, claims 8 and 18 are not made obvious by the combination of Shiell et al, Connor and Nishioka et al.

Claims 3 to 7 and 9 are allowable by dependence upon allowable base claim 1. Claims 12 to 17 are allowable by dependence upon allowable base claim 10.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. Thus no new search or reconsideration is required.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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